Advanced Control for Very Fast DC-DC Converters Based on Hysteresis of the C_{out} Current

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***Abstract*—The bandwidth achievable by using voltage mode control or current mode control in switch-mode power supply is limited by the switching frequency. Fast transient response requires high switching frequency, although lower switching frequencies could be more suitable for higher efficiency. This paper proposes the use of hysteretic control of the output capacitor (C_{out}) current to improve the dynamic response of the buck converter. An external voltage loop is required to accurately regulate the output voltage. The design of the hysteretic loop and the voltage loop are presented. Besides, it is presented a non-invasive current sensor that allows measuring the current in the capacitor. This strategy has been applied for DVS (dynamic voltage scaling) on a 5 MHz buck converter. Experimental results validate the proposed control technique and show fast transient response from 1.5 V to 2.5 V in 2 μs.**

***Index Terms*—DC-DC power conversion, dynamic response, non-linear circuits, transient response.**

I. Introduction

THIS WORK proposes an advanced control technique to optimize the dynamic response of very high frequency dc/dc converters to be integrated on a chip or in a package. A fast dynamic control technique can provide reduction in the size of the required output capacitors to meet the dynamic specs, making integration of the power converter easier. Several advanced control techniques have been presented in the literature with different approaches [1]–[18] to optimize the dynamic response of the buck converter. Control strategies like V^2 and hysteretic control of the output voltage [1]–[8] have received extensive attention because of the fast transient response and simple design. These techniques provide very good performance in applications where the equivalent series resistance (ESR) of the output capacitor is dominant, since the output voltage ripple is proportional to the current of the output capacitor. In applications where the ESR is not dominant, the use of these control strategies is limited. In [18], it is reviewed several ripple-based control techniques; V^2 and hysteretic control of the output voltage belongs to this type of techniques and also the control technique proposed in this paper. Most of the ripple based control techniques proposed in [18] measure the output voltage ripple adding a ramp to increase the robustness. However, the control proposed in this paper estimate the current through the capacitor that has direct information on the output current to react fast to load transients. In [19], it is proposed a sliding mode control where the output capacitor voltage and its derivative are used as state variables. The control technique proposed in this paper is similar to [19]. However, the derivative of the output capacitor voltage is the capacitor current only with ideal capacitors. In high frequency applications the ESL and the ESR are dominant and the derivative of the output voltage can not be considered the output capacitor current. In [9]–[12], time optimal digital controllers are presented. Although these techniques significantly improve the transient response, they suffer from having complex implementations. In [13], it is proposed a practical way to implement the "minimum time control," activating the non-linear control based on an estimation of the current; its main drawback is that it is digitally implemented and in order to have a fast transient response it is necessary to have a very high sampling rate.

The control strategy that is proposed in this paper [1], [2] overcomes the limitation of V^2 providing fast dynamic response even in applications where the ESR is not dominant. Additionally, the proposed control strategy is very suitable to change dynamically the output voltage. In the proposed strategy, the feedback of the output capacitor current is used to detect any change in the current load to response almost instantaneously; this is the key feature to achieve very fast dynamic response. The problem is to measure the output capacitor current but it can be estimated with a non-invasive method [3], [20] described in detail also in this paper.

The proposed control strategy is applied to a 5 MHz integrated converter. Thanks to the use of this control technique, the required output capacitance is 5 times smaller compared with the linear voltage mode control.

In Section II, the operating principle of the proposed control technique is presented. In Section III, the circuit used to estimate the current through the output capacitor is analyzed in detail and design guidelines are provided. Section IV shows how the required capacitors at the output of a 5 MHz integrated converters would be reduced thanks to this control approach. Finally, the presented control as well as the circuit that estimates the capacitor current is validated on a 5 MHz prototype in Section V.

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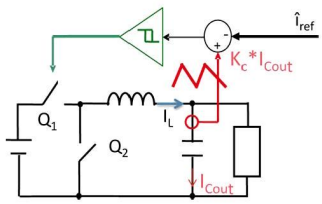


Fig. 1. Feedback of the current of the output capacitor.

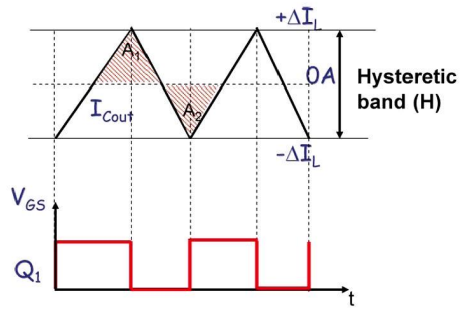


Fig. 2. Control concept. Steady state.

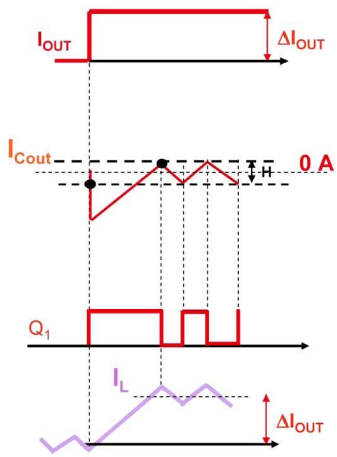


Fig. 3. Control concept. Transient response.

II. Scheme of the Proposed Control

The proposed control strategy is based on the combination of linear and non-linear control. The idea is to use the non-linear action to provide robustness for the control and also fast control action. Then, the slower linear loop provides accuracy and becomes less sensitive to noise and plant variations. In order to achieve fast transient response, the non-linear scheme is based on measuring the current of the output capacitor.

A. Control Concept

The idea is to switch the MOSFETs (Q_1 and Q_2) by means of the hysteretic control of the output capacitor current as shown in Fig. 1. The capacitor current is measured by a constant gain Kc. In steady state, the mean value of this current has to be zero (the area A_1 and A_2 are equal) since the output capacitor must be balanced (Fig. 2). The transient response under load steps relies on this non-linear loop. When a load step happens (Fig. 3), the capacitor current goes out of the hysteretic band and the duty cycle is saturated until the capacitor current comes back within the band. Hence, the response of this strategy under load step is really fast thanks to the hysteretic control.

This non-linear loop provides very fast response but an additional linear voltage loop (Fig. 4) is required to regulate the

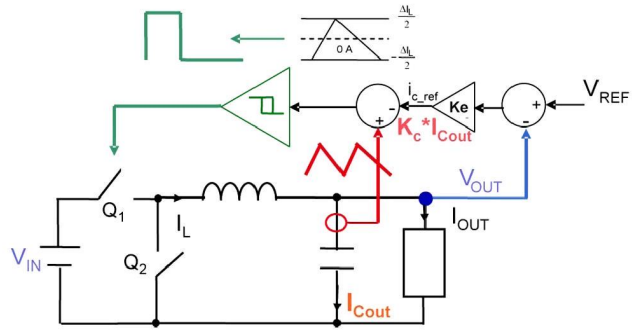


Fig. 4. Addition of a linear voltage loop.

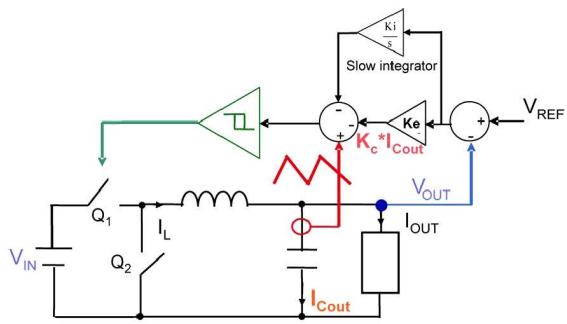


Fig. 5. Addition of a slow integrator for self-correction of the dc error.

output voltage at the specified dc point. The linear voltage loop provides the current reference for the non-linear loop and guarantees the zero dc value of the capacitor current. The output voltage regulation accuracy is also determined by this loop.

The main advantage of this hysteretic control of the capacitor current is that the fast dynamic response does not depend on a rapid change of the current reference under load or input voltage variations. Thus, the dynamic response is less sensitive to the slower linear voltage loop. A drawback of this control is that the switching frequency is variable.

The constant gain Ke of the voltage loop must be limited to avoid the amplification of the output voltage ripple and its interaction with the inner current loop. If Z_{Cout} is the magnitude of the impedance of the output capacitor, and considering the first harmonic of the voltage ripple, then, the non-interaction criterion is

$$\frac{Ke \cdot \Delta V_{pp}}{Kc \cdot \Delta I_L} \ll 1 \Rightarrow Z_{Cout}(f_{sw}) \cdot \frac{Ke}{Kc} \ll 1 \qquad (1)$$

B. DC Voltage Accuracy

There is dc error when the linear loop has to change the current reference after a variation in the load, input voltage or voltage reference. The dc error is given by (2).

$$error = \frac{i_{c\_ref}}{Ke} \qquad (2)$$

Regarding (2) when the current reference is zero the dc error becomes zero.

Although ideally there is no dc error, it could be introduced by the implementation. It can be easily corrected by adding an integrator in the voltage loop like shown in Fig. 5. The gain of the integrator should be low enough to avoid instabilities and the interaction with the inner loop.

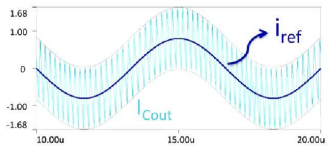


Fig. 6. Capacitor current follows a 150 kHz sinusoidal current reference.

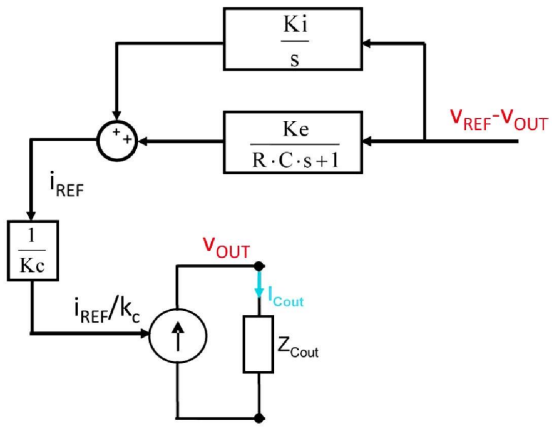


Fig. 7. Linear model to design the external voltage model.

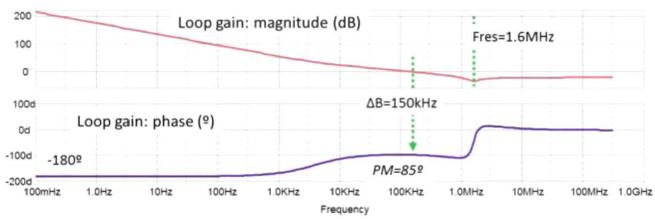


Fig. 8. Loop gain for the designed regulator: $Kc = 1$, $Ke = 3.77$, $Ki = 94200$, $RC = 100$ ns.

C. Voltage Loop Design and Stability Analysis

The buck converter together the hysteretic loop (Fig. 1) can be modeled by a current source that follows the reference current. Fig. 6 shows how in the circuit shown in Fig. 1, the capacitor current follows a 150 kHz sinusoidal current reference. Therefore, the circuit shown in Fig. 1 can be modeled by an average current source (Fig. 7), being this model valid for frequencies lower than $f_{sw}/10$. This linear model can be used to design the external voltage loop if the bandwidth is lower than $f_{sw}/10$.

The gain of the linear model (Figs. 7 and 8) is just the impedance of the output capacitor (in this case we are assuming that the load is inductive). The design of the regulator is very simple: 1) a pole $(1/(RCs+1))$ at the resonance frequency of the output capacitor is required to cancel the double zero that appears in the capacitor at this frequency, and 2) the gains Ke and Ki are adjusted to asses stability with a given bandwidth (smaller than $f_{sw}/10$).

In order to validate this simple linear model and also be able to analyze large signal instabilities, a deep model of the system, an implicit large-signal discrete map with variable sample time [21], is derived and used to analyze global stability and find the values of the state variables in steady state operation. The local stability is studied employing the Filippov's method [22]; if the singular values of the system are inside the circle of radius unity, then the system is locally asymptotically stable. Otherwise, it is unstable.

Based on this model, the stability of the system can be analyzed under different conditions. For example, it is analyzed

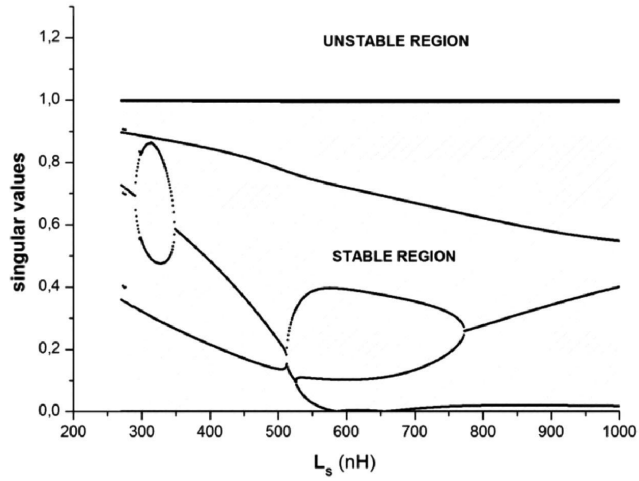


Fig. 9. Evolution of the singular values for $V_{OUT} = 1$ V. Sensor series inductance ranges from 270 nH up to 1000 nH.

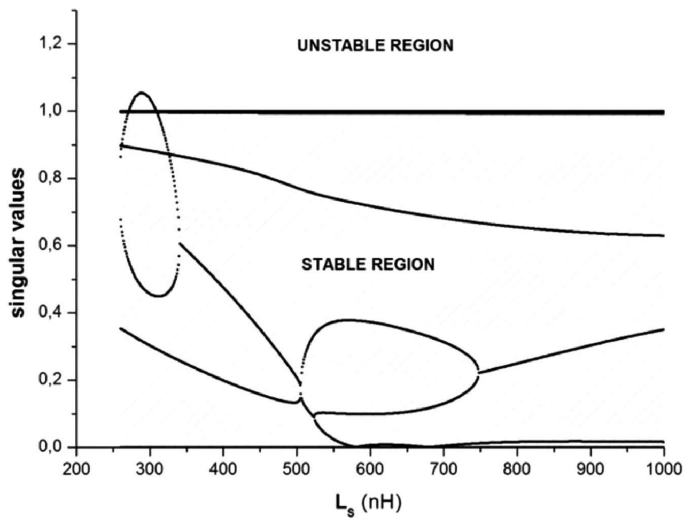


Fig. 10. Evolution of the singular values for $V_{OUT} = 2$ V. Sensor series inductance ranges from 270 nH up to 1000 nH.

how a mismatch in the series inductance of the current sensor (Ls) can affect the stability of the system. As explained in Section III, a mismatch between the output capacitor impedance and the sensor impedance can lead to instability problems.

For the system designed and tested in the experimental results, it has been analyzed how the sensor inductance (Ls) affects the stability of this system. It has been found that the system is stable for values higher than 270 nH, being the nominal value 450 nH. The system becomes unstable for values lower than 270 nH, -40% deviation from the nominal value, which is an extreme case; as it is presented in Section III, the series inductance of the sensor depends on the bandwidth of the op-amp, being its tolerance about $\pm 25\%$, which is a smaller value than the -40% variation required to create stability problems. Fig. 9 shows the evolution of the singular values of the system when the output voltage is 1 V. The system is locally stable for series inductances higher than 270 nH since all the singular values are lower than 1. Fig. 10 shows the same analysis when the output voltage is 2 V. It shows how at very low values of the series inductance, lower than 300 nH, the system becomes unstable since one singular value becomes higher than 1.

The linear model (Fig. 7) has been validated as a good and simple model to design the control loop. Then, the non-linear

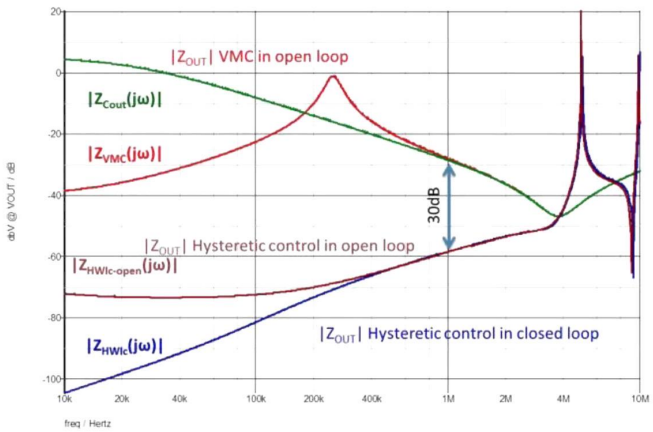


Fig. 11. Frequency response of a switched converter using Simplis-Simetrix.

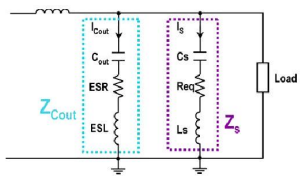


Fig. 12. Capacitor current sensing method (RLC network).

model can be used to deeply analyze the behavior of the designed system. For instance, in the linear model shown in Fig. 7, the current sensor is assumed to be ideal and it can not be used to analyze the instability effects due to mismatches of the sensor current.

D. Output Impedance

Fig. 11 shows the magnitude of the open loop output impedance of the VMC (red), the magnitude of the open loop output impedance of the hysteresis of the capacitor current (brown) and the magnitude of the closed loop output impedance of the hysteresis of the capacitor current (blue). The figure shows that the output impedance of the proposed control is very small. The simulation was obtained assuming same output filter (100 nH and 4 μF) for all the cases. The closed loop output impedance of the VMC becomes equal to the open loop output impedance at the bandwidth frequency. Therefore, if the bandwidth of the VMC is 1 MHz, being 5 MHz the switching frequency, the output impedance of the hysteresis control of the capacitor current is 30 dB smaller at 1 MHz frequency.

III. Capacitor Current Estimation: Analysis and Design Guidelines

The RLC network is a non-invasive method to measure the current of the output capacitor (C_{out}). The basic idea is to use an RLC network in parallel with the C_{out} (Fig. 12) to measure the current by scaling the impedance. The current in the parallel network of the output capacitor is proportional to the C_{out} current (Fig. 13). The figure shows that the sensor measurement (I_S) and the C_{out} current (I_{Cout}) have the same phases, same time constants and the impedance scaling.

A. Design of the Parallel RLC Network

The RLC network in parallel with output capacitor (to measure the current) is designed to present the same impedance than the output capacitor but scaled by a factor of n (Fig. 13). Therefore, the current through the parallel RLC network (I_S) is proportional to the output capacitor current (I_{Cout}) divided by the impedance scaling factor (n). Equations (3)–(5) should be accomplished in order to design an appropriate RLC network.

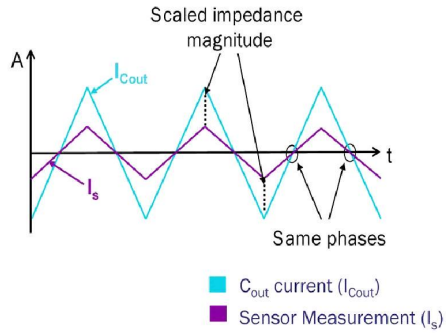


Fig. 13. Matched phases and impedance scaling between sensor current (I_S) and C_{out} current (I_{Cout}).

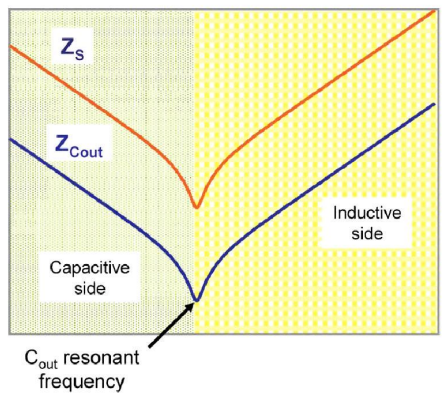


Fig. 14. Impedance of the output capacitor (Z_{Cout}) and impedance of the parallel RLC network (Z_S).

$$Cs = \frac{C_{out}}{n} \tag{3}$$

$$Req = n \cdot ESR \tag{4}$$

$$Ls = n \cdot ESL \tag{5}$$

Fig. 14 shows the impedance of the output capacitor (Z_{Cout}) and the impedance of the parallel RLC network (Z_S). The figure shows that both impedances have the same behavior, but scaled by a factor n.

B. Sensor Operation

The proper operation of this sensor strongly depends on the relative position of the converter switching frequency (f_{sw}) and the C_{out} resonant frequency (f_{res}). If $f_{sw} > f_{res}$, the C_{out} impedance presents inductive behavior (Fig. 15). When $f_{sw} < f_{res}$, the impedance is capacitive. If the sensor is designed for the inductive side, f_{res} must always be lower than f_{sw} to guarantee the appropriate operation.

The selected output capacitor for the prototype has the following features: $C_{out} = 4$ μF, $ESR = 4.5$ mΩ, $ESL = 450$ pH, $f_{res} = 3.77$ MHz. Since the switching frequency of the converter is 5 MHz, the C_{out} impedance presents inductive behavior ($f_{sw} > f_{res}$).

C. Physical Implementation: Trans-Impedance Amplifier

The actual implementation of the RLC network is based on a trans-impedance amplifier (Fig. 16). The main advantage of this circuit is that it allows to model the ESL effect which is very

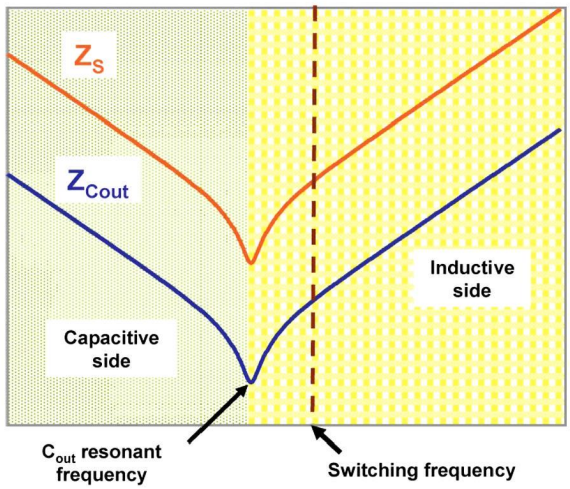


Fig. 15. Sensor operation: inductive side.

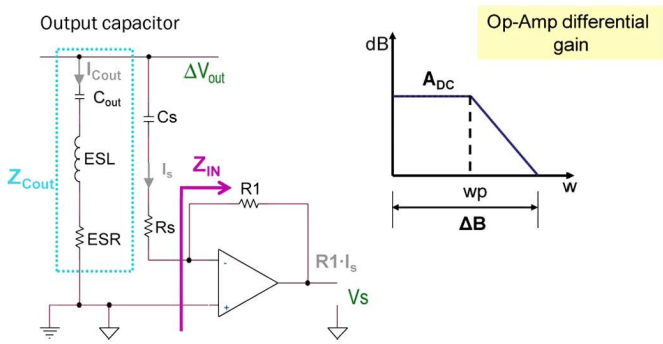


Fig. 16. Physical implementation of the capacitor current sensing method (RLC network).

important at high frequency operation. The op-amp frequency behavior is assumed as a dc gain (A_{dc}) with a pole at wp, being ΔB the op-amp bandwidth (Fig. 16). The gain of the sensor (Kc) is approximately given by (6).

$$Kc = -\frac{R1}{n} = \frac{\Delta Vs}{\Delta I_{Cout}} \tag{6}$$

The input impedance of the trans-impedance amplifier behaves as a resistive (Ri) and inductive (Ls) series network (Fig. 17). This inductive [see (7)] behavior is required to match the ESL effect of the output capacitor (assuming that $f_{sw} < \Delta B/10$). The input resistance (Ri) behavior [see (8)] of the trans-impedance amplifier is required to match Rs with the Req of the RLC network. The relationship between the Req, Ri and Rs is given by (9).

$$Ls = \frac{R1}{\Delta B} \tag{7}$$

$$Ri = \frac{R1}{A_{dc}} \tag{8}$$

$$Rs = Req - Ri \tag{9}$$

The design of this current sensor is sensitive to tolerances of bandwidth and dc gain of the op-amp. Fig. 18 shows the range of ΔB and A_{dc} variation for a specific op-amp (AD8061). For example, -15% ΔB tolerance of the op-amp generate -15% f_{sw} variations. The temperature also modifies the bandwidth of the op-amp. For example, decrement of temperature (from 25 °C to -55 °C) results on approximately $+6.4\%$ of ΔB increment. An increment of temperature (from 25 °C to 125 °C) results

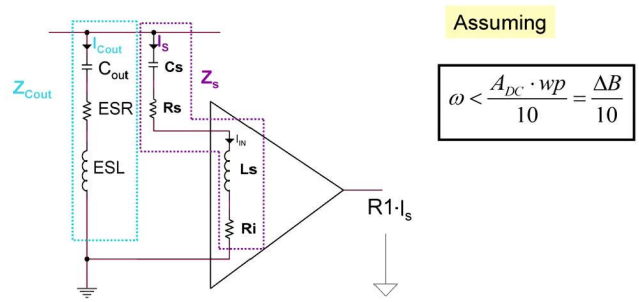


Fig. 17. Equivalent circuit of the trans-impedance amplifier. The input impedance of the op-amp presents inductive behavior (Li).

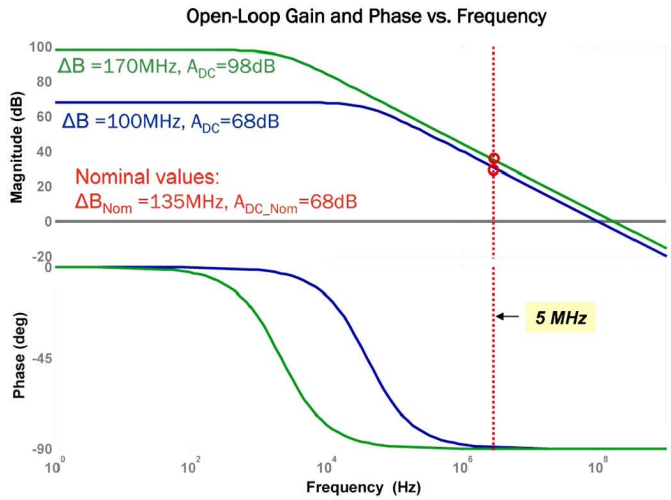
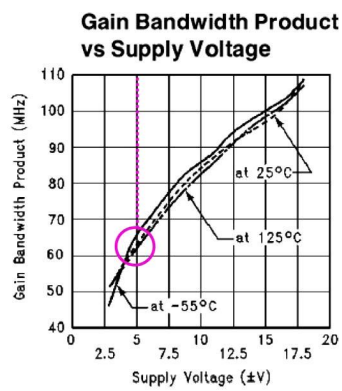


Fig. 18. Frequency response of op-amp: AD8061. Maximum and minimum bandwidth and A_{dc} according to data sheet.



ΔB variation (Temperature)= +6.4% ΔB (decrement from 25°C to -55°C) and -1.6% ΔB (increment from 25°C to 125°C).

Fig. 19. Tolerance of the op-amp bandwidth. LM6171.

on approximately -1.6% of ΔB decrement. Fig. 19 shows for a specific op-amp (LM6171) how the temperature affects the value of the ΔB.

D. Determine the Appropriate Op-Amp

The selection of the op-amp should accomplish the limits of the ΔB and Kc in order to maintain the sensor working in the same side, either inductive or capacitive.

1) Determine the ΔB_{Min}*:* The characteristics of the selected op-amp should accomplish: the minimum value of the bandwidth (ΔB_{Min}) that guarantees the internal stability and the ideal gain of the op-amp $(Vs/I_S = -R1)$.

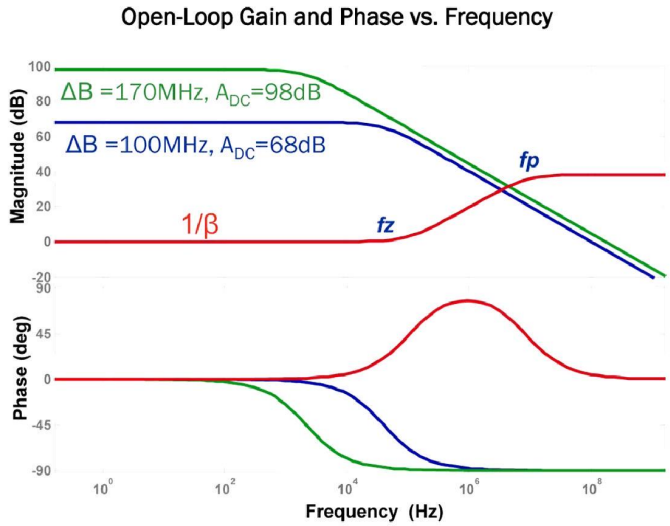


Fig. 20. Op-amp: Internal stability analysis.

D.1.1) The design must guarantee the internal stability of the op-amp (Fig. 20). For this design example the Kc value is equal to 1/2.56 V/A. The selected op-amp is AD8061, the nominal ΔB is equal to 135 MHz and the A_{dc} is equal to 68 dB.

The closed loop gain $(1/\beta)$ of the trans-impedance amplifier is given by (10) and the corresponding pole (fp) and zero (fz) of the transfer function are shown in (11). The fz and fp values do not depend on the value of the impedance scaling "n". Therefore, for a given C_{out} (C_{out}, ESL and ESR) and f_{sw}, fp and fz are fixed.

$$\beta^{-1} = \frac{(R1 + \mathrm{Rs}) \cdot \mathrm{Cs} \cdot s + 1}{\mathrm{Rs} \cdot \mathrm{Cs} \cdot s + 1} \tag{10}$$

$$fz = \frac{1}{2 \cdot \pi \cdot (R1 + \mathrm{Rs}) \cdot \mathrm{Cs}}$$

$$fp = \frac{1}{2 \cdot \pi \cdot \mathrm{Rs} \cdot \mathrm{Cs}} \tag{11}$$

D.1.2) The selected op-amp should accomplish the minimum value of the bandwidth (ΔB_{Min}) that guarantees the ideal gain of the op-amp. The value of Kc should be chosen in order to asses that the gain at the switching frequency of the trans-impedance amplifier is approximately the ideal gain $(Vs/I_S = -R1)$. The real gain of the sensor (Kc) is approximately given by (12). At the switching frequency, it is necessary to guarantee that $R1 \gg Z_{IN}(f_{sw})$; this condition is met if $f_{sw} < \Delta B/10$. Therefore the op-amp must have high bandwidth, penalizing the consumption of the op-amp.

$$Kc(f_{SW}) = \frac{Z_{IN}(f_{SW}) - R1}{n} \approx -\frac{R1}{n} \tag{12}$$

2) Determine the ΔB_{Max}: The maximum value of the bandwidth (ΔB_{Max}) should accomplish that the resonant frequency of the sensor (f_{res_sensor}) should be less than the switching frequency (f_{sw}), keeping the sensor operation in the inductive side (see Fig. 21).

It is important to highlight that for a selected op-amp the gain of the sensor (Kc) is fixed and it does not depend on the n value. Taking into account (5), (7), and (12), it is obtained that $Kc = -ESL \cdot \Delta B$.

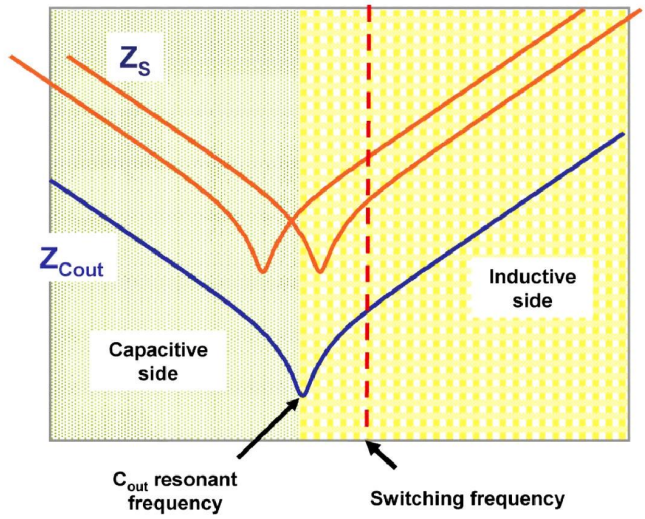


Fig. 21. Impedance of the C_{out} and variation in the impedance of the parallel RLC network.

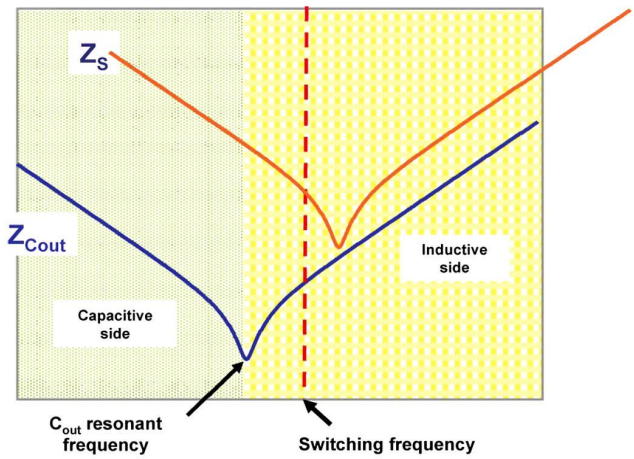


Fig. 22. System limitation. Impedance of the output capacitor (Z_{Cout}) and impedance of the parallel RLC network (Z_S).

E. Sensor Limitation

The proper operation of this sensor strongly depends on the relative position of the converter switching frequency (f_{sw}) and the C_{out} resonant frequency (f_{res}). If the impedance behavior of C_{out} is different than expected (capacitive instead of inductive) due to the tolerance effects, the phase of the current changes dramatically producing malfunctioning of the sensor (Fig. 22). Fig. 23 shows a sensor designed for the inductive side, but if C is smaller (in this case 50% smaller) than expected, the system changes from inductive to capacitive side. As a result of this C reduction: the real and measured currents are no longer in phase. Therefore, it is necessary to assure by design that the system always operates in the same side.

1) Parameters That Modify the Resonant Frequency: The capacitance is the output capacitor parameter most sensitive to tolerance effects like aging and dielectric material tolerances. The dielectric material affects the capacitance value in multilayer ceramic chip (MLCC) capacitor. For example, using X7R dielectric material tolerance is $\pm 10\%$, X5R changes $\pm 20\%$ and Y5V changes $+80\%$ and -20% of the capacitance value. These capacitance tolerances affect the resonant frequency. For example, for X7R dielectric material, Kyocera capacitor presents a -26% reduction in capacitance value due to aging and temperature effects. This variation increases the resonant frequency

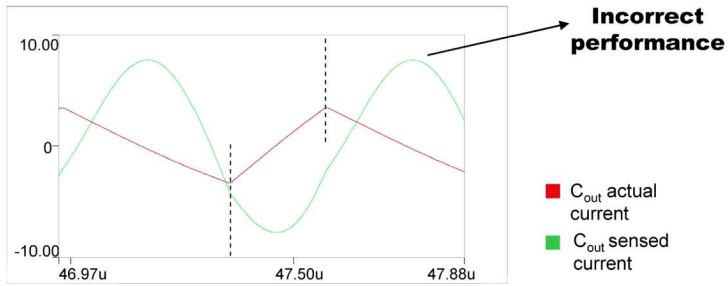


Fig. 23. Measurement failure. Sensor designed for the inductive side, but C is smaller than expected.

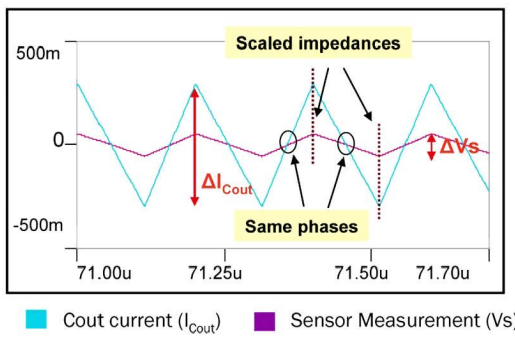


Fig. 24. Simulation of designed sensor. Same phase, time constants and impedance scaling between Vs and I_{Cout}. Sensor designed for 135 MHz and A_{dc} of 68 dB.

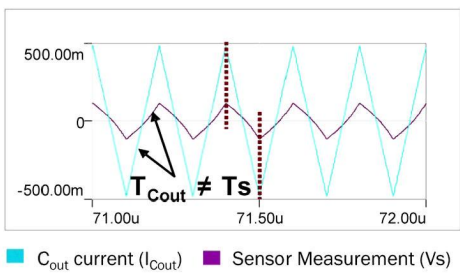


Fig. 25. Effect of a mismatch in op-amp bandwidth: Nominal $\Delta B = 135$ MHz, simulated $\Delta B = 100$ MHz.

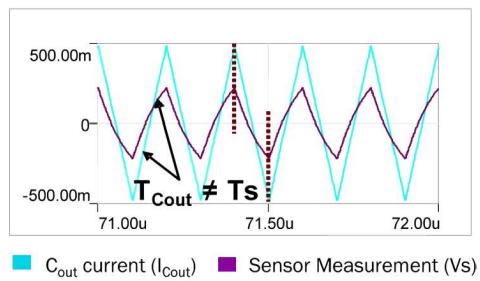


Fig. 26. Effect of a mismatch in op-amp bandwidth: Nominal $\Delta B = 135$ MHz, simulated $\Delta B = 170$ MHz.

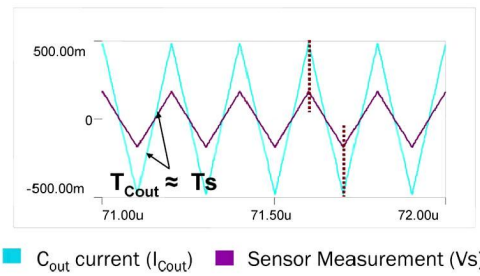


Fig. 27. Effect of a mismatch in op-amp dc gain: Nominal $A_{dc} = 68$ dB, simulated $A_{dc} = 98$ dB.

1.15 times higher (from 1.59 MHz to 1.8 MHz). In [3], it is analyzed in more detail the parameters that affect the switching frequency.

F. Simulation Results and Tolerance Analysis (Influence of Different ΔB and A_{dc})

The specifications for the example are: $V_{IN} = 4$ V, $V_{OUT} = 1$ V, $C_{out} = 4$ μF, $ESR = 4.5$ mΩ, $ESL = 450$ pH and $f_{sw} = 5$ MHz. The parallel RLC network is composed of $Cs = 400$ pF, $Ls = 4.4$ μH, $Req = 48$ Ω, $R1 = 3.7$ kΩ, $Ri = 1.5$ Ω and $Rs = 47$ Ω. The "n" value for the design example is equal to 10000. The trans-impedance amplifier used for the current sensor design is AD8061 ($\Delta B = 300$ MHz). The design methodology is validated by simulation. The influence of the variation of ΔB and A_{dc} in the performance of the sensor has also been analyzed by simulation. These variations produce different time constants between the sensed current and C_{out} current. In spite of these variations a robust system is obtained. Fig. 24 shows the validation of the current sensor design, this validation is done by simulation, it shows that both signals are in phase, scaled amplitudes and the peaks of the waveforms are in phase.

However, the design of this current sensor is sensitive to tolerances of bandwidth and dc gain of the op-amp. Figs. 25 and 26 show the simulation results of a current sensor designed with an op-amp whose nominal bandwidth is $\Delta B = 135$ MHz and its tolerance is $\pm 26\%$, hence, the minimum ΔB of the op-amp is 100 MHz and the maximum is 170 MHz. These figures show that different bandwidth produces different constant times, but the peaks of the triangular waveform are in phase (Figs. 25 and 26). Finally a variation in dc gain of the op-amp produces a negligible effect in Kc value (Fig. 27).

The previous analysis is focused on the tolerances of the current sensor (Cs, Req, and Ls) but the analysis is completely applicable to tolerances of the output capacitor (C_{out}, ESR, and ESL). What is really important is the relative mismatch between the impedance of the sensor and the impedance of the capacitor. The variation of the capacitance is not considered because in this case the system is operating in the inductive side of the output capacitor and the sensor; variations in the capacitance values of C_{out} or Cs would not affect the operation since the impedance at the switching frequency is dominated by the inductive behavior.

IV. 5 MHz Integrated Converter

In this section, an analysis of the C_{out} size reduction applied to a commercial dc-dc converter (EN5365QI) is presented. Fig. 28 shows a picture of a dc-dc converter manufactured by Enpirion, Inc. The EN5365QI is a 6 A voltage-mode synchronous buck converter operating at 5 MHz where the output inductor is in the same package and linear control is used. The required output capacitors to meet the dynamics specifications are placed outside. Fig. 29 shows that under a 6 A load steps

Fig. 28. EN5365QI. 5 MHz Synchronous buck converter.

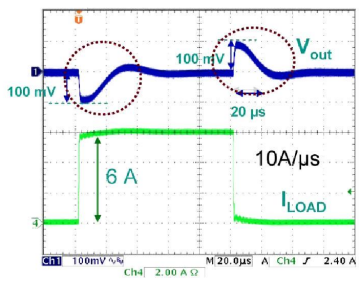


Fig. 29. EN5365QI. Regulation under 6 A (10 $\mathbf{A/\mu s}$) load step (20 $\boldsymbol{\mu s/div}$). $V_{IN} = 5.5$ V, $V_{OUT} = 3.3$ V and $C_{out} = 50$ μF.

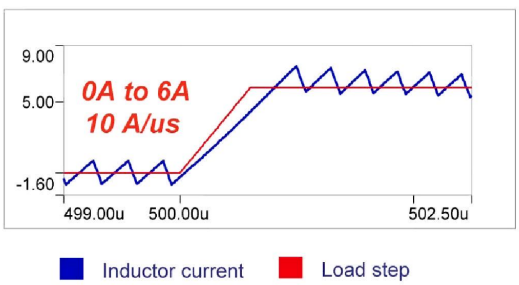


Fig. 30. Inductor current response under a 10 $\mathbf{A/\mu s}$ load step (0 A to 6 A).

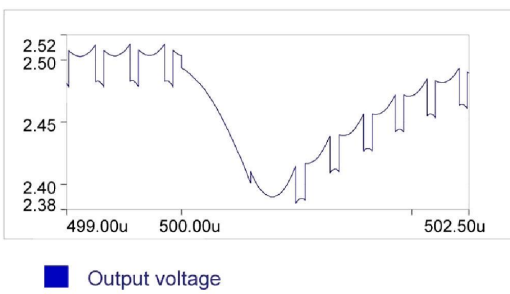


Fig. 31. Output voltage deviation under 10 $\mathbf{A/\mu s}$ load step (0 A to 6 A).

the output voltage deviation is approximately 100 mV ($\pm 3\%$ of the V_{OUT}).

The input specifications for the analysis are: load step from 0 A to 6 A with 10 $\mathbf{A/\mu s}$, maximum output voltage deviation of $\pm 5\%$ of the V_{OUT}, $V_{IN} = 3.3$ V and $V_{OUT} = 2.5$ V. The output capacitor that satisfy the maximum output voltage deviation is $C_{out} = 5 \times 10$ μF, being the equivalent $ESR = 0.6$ mΩ and the equivalent $ESL = 0.9$ nH and the resonance frequency about 0.75 MHz.

Figs. 30 and 31 show the simulations results for $C_{out} = 1 \times 10$ μF, $ESL = 1$ nH and $ESR = 2$ mΩ (resonance frequency ≈ 1.6 MHz). Fig. 30 shows a load step from 0 A to 6 A under 10 $\mathbf{A/\mu s}$. Fig. 31 shows that under a 6 A load steps the output voltage deviation is 120 mV (-4.7% of the V_{out}).

The simulation results demonstrate that the proposed control technique reduce the size of the C_{out} (from 5×10 μF to 1×10 μF) and meets the specifications of the output voltage deviation

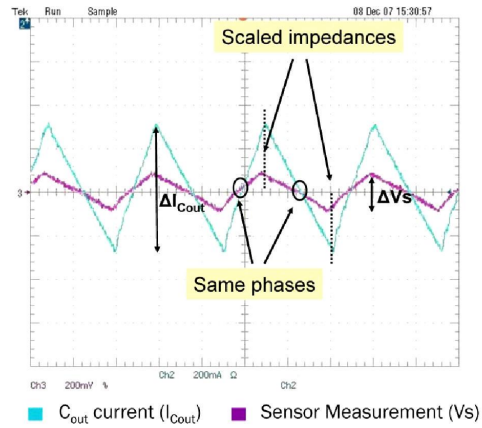


Fig. 32. Experimental measurement of sensor. Waveforms for the V_S and I_{Cout} have the same time constants and scaled magnitudes.

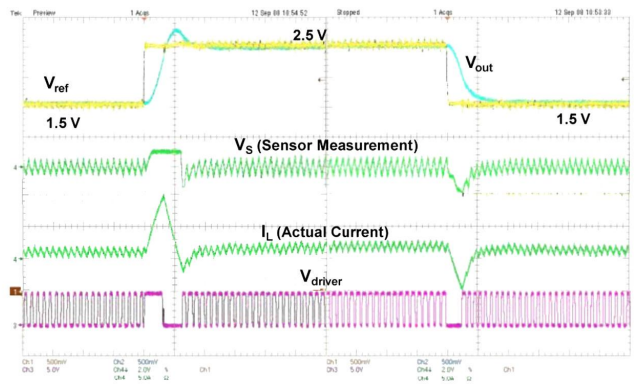


Fig. 33. Voltage step (V_{ref}) from 1.5 V to 2.5 V within 2 μs (1 $\boldsymbol{\mu s/div}$), V_{out} (500 mV/div), V_S (2 A/div), I_L (5 A/div).

($\pm 5\%$ of the V_{out}). The frequency ripple in both cases (5×10 μF and 1×10 μF) should be similar since the inductive behavior is dominant at the switching frequency (5 MHz).

V. Experimental Results

A discrete buck converter switching at 5 MHz is built to validate the concept. The power stage is properly designed for variable output voltage and load step regulation with the guidelines given in [15]. The buck converter is designed to meet 2 μs transitions from 1.5 V to 2.5 V, tight regulation (50 mV) under aggressive 1 A load steps, output voltage ripple less than 8 mV, and very small size. These specifications are met with a one phase Buck with a 100 nH inductor and fast switching MOSFETs. The output capacitance is only 4 μF.

The gain ratio of the loops is designed according to (1). Fig. 32 validates the design methodology of the current sensor design. It also shows that the sensor measurement (V_S) and the I_{Cout} current are in phase, scaled amplitudes and the peaks are in phase.

The tracking of the voltage reference is shown in Fig. 33. The transition time is 2 μs, which is close to the minimum transition time for the power stage design. V_S is the output of the current sensor and it shows an appropriate current measurement for a fast transient response. Therefore, experimental results validate the current sensor design for a very fast transient response.

The regulation under 45 $\mathbf{A/\mu s}$ load step is shown in Fig. 34. Under a 2.5 A load steps the output voltage deviation is approximately 60 mV being the output capacitance only 4 μF

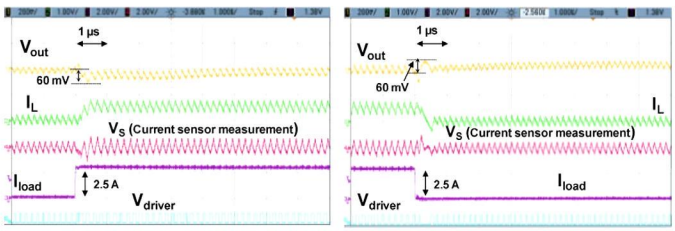


Fig. 34. Regulation under 2.5 A (45 $\mathbf{A/\mu s}$) load step (1 $\boldsymbol{\mu s/div}$).

($4 \times 1\ \mu\mathbf{F}$). Fig. 34 shows no dc error since there is an integration action in the voltage loop. This figure also shows that under load step the output voltage recovers the steady state within 1 $\boldsymbol{\mu s}$.

VI. Conclusions

A control strategy based on the combination of a hysteretic control of the capacitor current with an outer voltage loop is proposed to increase the effective bandwidth over the MHz range in a Buck converter. The hysteretic control provides a very fast control action for load and output voltage steps. The voltage loop provides accuracy in steady state conditions.

This control strategy is based on the feedback of the output capacitor current. The control achieves very fast response for load steps and near minimum transition time for output voltage steps. The outer voltage loop becomes a first order system which can be compensated easily. The design of the hysteretic loop and the voltage loop (based-on stability and dynamic response issues) is presented and validated by simulations and experimentally. These loops are designed to guarantee no interaction among them. A non-invasive current sensor is presented, it enables the fast transient response of the proposed technique but at the same time, the sensitivity to the mismatch of the component values becomes the main drawback, being more appropriate for applications where the output capacitor is known. This control strategy is validated with the design of 5 MHz buck converter for dynamic voltage scaling and tight regulation under load steps. Experimental results show a very fast dynamic response in Buck converter (step voltage of 1.5 V to 2.5 V and from 2.5 V to 1.5 V in 2 $\boldsymbol{\mu s}$). Also, the response of the current sensor under load and voltage steps is experimentally validated.

The proposed control technique would allow to divide by 5 (from $5 \times 10\ \mu\mathbf{F}$ to $1 \times 10\ \mu\mathbf{F}$) the required output capacitance in a commercial 5 MHz integrated converter. The main applicability of the proposed control technique is for fast-dynamics high-switching frequency converters where the output capacitor is known. Another specification that benefits these techniques in front of others is applications where there is very small room for the output capacitors, being ceramic the more appropriate capacitors to be used (i.e., integrated dc/dc converters: power on chip or power on package).

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